APPLICATION FOR UNITED STATES PATENT

Inventor(s): LEE, Hee-Chun

Invention: SUBSTRATE BIAS GENERATOR IN SEMICONDUCTOR MEMORY DEVICE

Cushman Darby & Cushman, L.L.P.
1100 New York Avenue, N.W.
Ninth Floor, East Tower
Washington, D.C. 20005-3918
Attorneys
Telephone: (202) 861-3000

SPECIFICATION

3

376347 A/NO fee

08/691822

SUBSTRATE BIAS GENERATOR IN SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device, and more particularly to a substrate bias generator which makes device characteristics stable by supplying a predetermined negative voltage to a substrate and minimally reduces current consumption during a self refresh mode.

In general, a P-type substrate is employed in a dynamic RAM having a memory cell which is composed of one access transistor and one storage capacitor. Further, it is well known that a substrate bias generator must be included in the use of the P-type substrate, the substrate bias generator supplying a negative voltage of a predetermined level to the substrate. ~~In the meantime, the~~ The substrate bias generator is installed ~~in~~ inside of a chip and the negative voltage is thus provided to the substrate because ~~there are~~ the following ~~some advantages,~~ advantages as compared with a case of connecting the substrate to a ground terminal GND. First, it ~~is~~ possible to minimize variation of a threshold voltage generated by body effect of a transistor and ~~it is possible~~ to obtain efficiency of operational speed by making a punch-through voltage high and by reducing a junction capacitance. Second, ~~in order to protect~~ the biased substrate protects the memory device, ~~it is possible to suppress~~ by suppressing forward-bias by reducing sub-threshold current and by undershooting an input voltage of TTL(Transistor-Transistor Logic) input stage. According to the above advantages, if ~~the~~ constant negative voltage (bias) is provided to the substrate by the substrate voltage generator, the function of the memory device is generally improved.

~~In the meantime, the~~ A substrate bias generator ~~of~~ in which driving capacity is improved is disclosed in U.S. Patent No. 5,157,278 entitled "Substrate Voltage

Generator for Semiconductor Device" granted on 20 October 1992. Fig. 1 is a schematic block view showing a substrate bias generator disclosed in the above U.S. Patent No 5,157,278. Fig. 1 is composed of a voltage pump circuit 6 providing a substrate bias voltage VBB, a substrate voltage level detector 10 detecting the voltage level of the substrate bias voltage VBB, a signal delay circuit 2 delaying an output signal of the substrate voltage level detector 10 during a predetermined time and thereby generating the output signal, and an oscillator 4 performing an oscillating operation in response to the output signal of the signal delay circuit 2 and driving the voltage pump circuit 6. In such a construction, if the oscillator 4 is operated, the substrate bias voltage VBB is synchronized with an oscillating signal ϕOSC generated in the oscillator 4 and is boosted to a predetermined negative voltage by the voltage pumping operation of the voltage pump circuit 6. ~~In the meantime, the~~ substrate voltage level detector 10 shown in a dotted line ~~block~~ block of Fig. 1 includes a PMOS transistor 12 having a channel formed between a power supply terminal Vcc and a connecting node 14 and ~~being~~ which is always ~~apt to be~~ turned on, a PMOS transistor 16 whose source terminal is connected to the connecting node 14 and whose gate terminal is connected to the substrate bias voltage VBB, an NMOS transistor 18 having the channel formed between the PMOS transistor 16 and a ground terminal Vss and ~~being~~ which is always ~~apt to be~~ turned on, and an inverter 20 having an input terminal coupled to the connecting node 14 and driving the signal delay circuit 2. The substrate voltage level detector 10 detects the level of the substrate bias voltage VBB and controls the oscillator 4 in response to such a detecting operation. Therefore, in the case that the voltage level of the substrate bias voltage VBB is over a desired negative voltage level (in this case, an absolute value of the substrate bias voltage VBB is too small), the substrate voltage bias VBB is boosted to the desired negative voltage level by generating a signal to enable the oscillator 4 and by operating the oscillator 4. On the other hand, in the case that the voltage level of the substrate voltage VBB is below the desired negative voltage level (in this case, the absolute value of the substrate bias voltage VBB is too large), the substrate bias voltage VBB is continuously maintained at the desired negative voltage level by generating the signal to enable the oscillator 4 and by stopping the operation of the oscillator 4. The signal delay circuit 2, which receives ~~2 receiving~~ the output signal of the substrate voltage level detector 10, prevents the voltage level of the substrate bias voltage VBB from being sensitively varied and thereby makes the operation of the substrate bias generator stable.

In the construction of the substrate voltage level detector 10 detecting the voltage level of the substrate bias voltage VBB, the PMOS transistor 16 is switch-controlled by the substrate bias voltage VBB according to a gate-input of the substrate bias voltage VBB. Accordingly, if the bias voltage level of the substrate voltage VBB becomes high, too the voltage level charged to the connecting node 14 is raised. The inverter 20 is output at the "low" level. In this case, the oscillator 4 is enabled. On the other hand, if the voltage level of the substrate bias voltage VBB becomes too low, the voltage level charged to the connecting node 14 is dropped. The inverter 20 is output at the "high" level. In this case, the oscillator 4 is disabled. The substrate bias voltage VBB softly or heavily ~~turns~~ turn on the channel of the PMOS transistor 16, however, it ~~can~~ cannot completely ~~not~~ turn off the channel thereof. Therefore, the PMOS transistors 12 and ~~14~~ 16 and the NMOS transistor 18 are always turned-on, so that a direct current flows between the power supply terminal Vcc and the ground terminal Vss. Further, the voltage level charged to the connecting node 14 is set near a trip point of the inverter 20, so that ~~the other~~ another direct current flows between the power supply terminal Vcc and the ground terminal Vss in the inverter 20(this is generally composed of a CMOS inverter). Therefore, ~~the~~ a current of the substrate voltage level detector 10 always flows ~~in case of powering up of~~ when the chip is powered up regardless of the operation of the semiconductor memory device. This ~~specially~~ causes ~~the consumption of the~~ operational current ~~to be increased~~ during a stand-by state.

~~In the meantime, in~~ In the case of ~~the cell which has the~~ a cell which has a dynamic construction such a dynamic RAM, it is well known that a refresh mode is included as one operational mode in the semiconductor memory device so as to perform a rewrite operation of cell storage data. ~~In special, a~~ A self refresh mode is generally employed in the semiconductor memory device, the self refresh mode performing a refresh operation according to an interval of constant time. The dynamic RAM ~~performing low current consumption~~ consumes a low amount of current as during the self refresh mode, is disclosed ~~in~~ on pages 43 to 44 of a paper from ~~"1993~~ the 1993 Symposium on VLSI circuits, entitled "Low power Self Refresh Mode With Temperature Detecting Circuit". As is well known, the self refresh mode is divided into active and stand-by states. The active and stand-by states of the self refresh mode have a constant interval, respectively. The interval is determined ~~in~~ during the design of the chip. Accordingly, it is well known that the stand-by state of the self refresh mode is generated at

a constant interval unlike that of the chip, and that the stand-by state thereof is ~~longer~~ maintained longer than the active state thereof (actually, the stand-by state occupies most of the self refresh mode). This is well known from the above paper or from data books of Samsung Co., Ltd. published 1992 and 1993. As mentioned above, during the stand-by state of the self refresh mode, ~~the~~ a direct current flows into the ground terminal Vss from the power supply terminal Vcc in the substrate voltage level detector 10, thereby generating ~~the~~ constant current consumption. On the other hand, in the case that the time length of when the semiconductor memory device is ~~stayed~~ held in the stand-by state is similar to or is shorter than the operational period of the substrate bias generator, during the stand-by state, the substrate bias generator doesn't need to operate, ~~however,~~ only during the active state, it should operate. Thereby, ~~the~~ current consumption according to the substrate voltage is prevented from being increased during the stand-by state. However, since the length of time of the stand-by state is not determined in the operation of the general semiconductor memory device, it is impossible to reduce the current consumption under the stand-by state according to the above method. In the self refresh mode to be refreshed by a fixed period designed into ~~the period of~~ the chip, since the time when the semiconductor memory device is ~~stayed~~ held in the stand-by state and the active state is determined by the period generated in ~~inside of~~ the chip, it is possible to know the length of time when the semiconductor memory device is ~~stayed~~ held in the stand-by state. Nevertheless, the current consumption generated in the chip is in ~~total~~ increased according to the current consumption generated from the substrate voltage level detector 10 during the stand-by state of the self refresh mode. It has been estimated that such increase of the current consumption can interfere with the suppression of the power consumption in the superhigh integrated semiconductor memory device having an otherwise low power.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a substrate bias generator implementing a semiconductor memory device which consumes low power.

It is another object of the present invention to provide a substrate bias generator of a semiconductor memory device which ~~minimally~~ reduces current

to a minimum
consumption during a self refresh mode.

It is still another object of the present invention to provide a substrate bias generator in which current consumption is prevented from being generated during a stand-by state of the self refresh mode.

It is a further object of the present invention to provide a substrate bias generator capable of preventing ~~inside of~~ a substrate voltage level detector from ~~generation of~~ consuming direct current during the stand-by state of the self refresh mode.

It is still a further object of the present invention to provide a substrate bias generator capable of reducing current consumption of a semiconductor memory device by preventing ~~inside of~~ a substrate voltage level detector from ~~generation of the~~ consuming direct current during the stand-by state of the self refresh mode.

It is yet another object of the present invention to provide a substrate bias generator of a semiconductor memory device capable of reducing current consumption by stopping ~~an~~ a substrate voltage detecting operation during the stand-by state, the semiconductor memory device ~~having as an operational mode the~~ including a self refresh mode which is divided into active and stand-by states.

The present invention according to the above objects is to provide a substrate bias generator to supply ~~an~~ a negative voltage to a substrate of the semiconductor memory device having ~~the~~ a self refresh mode.

The substrate bias generator according to the present invention has a substrate voltage level detector. ~~As the~~ The substrate voltage level detector ~~synchronizes~~ is synchronized with the period of the self refresh operation during the self refresh mode such that the substrate voltage level detecting operation is enabled during the active state of the self refresh mode, ~~whereas~~ and it is disabled during the stand-by state thereof.

The substrate voltage level detector according to the present invention comprises an input terminal for inputting an active signal of the self refresh mode and a switching device for controlling the substrate voltage level detecting

operation of the substrate voltage level detector by being switch-controlled in response to an output level of the input terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the present invention will be more apparent from the following detailed description taken with the attached drawings in which:

Fig. 1 is a schematic block view of a substrate bias generator according to ~~a~~ conventional art;

Fig. 2 is a schematic block view of a substrate bias generator according to the present invention;

Fig. 3 is a detailed circuit view showing embodiments of a substrate voltage level detector 26 and its controller 28 according to the block construction of Fig. 2; and

Fig. 4 is a timing diagram of ~~each of~~ signals generated by the circuit of Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

~~The point of the description of the preferred embodiment of the present invention is that a~~ substrate bias generator ~~is to prevent the consumption~~ current ~~generated~~ thereby during a stand-by state of a self refresh mode. Therefore, for convenience of the explanation, in the following description, a term "active state" is defined as that of the self refresh mode and ~~another~~ the term "stand-by state" is determined where otherwise noted such as in ~~as~~ that of the self refresh mode, except a ~~determined~~ case like an "active state of a chip" or a "stand-by state of the chip". Further, a signal ϕself of signals mentioned hereinafter indicates an enable signal and another signal ϕact thereof indicates an active signal of the self refresh mode.

Fig. 2 is a schematic block view of the substrate bias generator having a substrate voltage level detector according to the present invention. In the construction shown in Fig. 2, a portion indicated by a dotted line block, is a new construction according to the present invention and is the subject matter of the present invention. Since the rest of portions except the dotted line block portion are the same as those of Fig. 1, their reference numerals are also the same as

those of Fig. 1. In synchronization with the period of the self refresh operation, the detecting operation of the substrate voltage level detector 26 is enabled during the active state, whereas it is disabled during the stand-by state. Such a detecting operation is determined by the substrate voltage level detecting controller 28 which controls the substrate voltage level detector 26 by inputting in a feed-back manner the self refresh enable signal ϕself, the active signal ϕact of the self refresh mode and an output signal of the substrate voltage level detector 26. Accordingly, the driving capacity of the substrate voltage level detector 26 is determined according to the control of the controller 28 and will be explained in detail ~~explained~~ hereinafter.

~~In the meantime, in~~ In order to more easily understand the present invention, the self refresh mode and the current consumption thereunder will be explained as follows. As is well known in the art, the level of the substrate bias voltage VBB is raised by junction leakage current and substrate current caused by hot ~~carrier~~ carriers generated when the transistors are operated. Therefore, ~~in case that~~ in the case when the semiconductor memory device is not operated and only power is provided, i.e., during the stand-by state of the chip, ~~there is scarcely~~ the substrate current is scarcely generated by the operation of the transistor and there remains only the junction leakage current. Thereby, the oscillator is operated during the stand-by state of the chip. If the semiconductor memory device is ~~at~~ in the active state ~~of the chip~~, many transistors are operated to generate a large amount of substrate current, so that the substrate bias voltage VBB is raised and the operating time of the substrate bias generator becomes long. Accordingly, during the stand-by state of the chip, the operational period of the substrate bias generator is determined depending upon the driving capacity of the voltage pumping circuit, i.e., depending upon how soon the substrate bias voltage VBB is charged up to the operational level of the oscillator by the junction leakage current and how soon it is dropped to the desired level. In the stand-by state of the chip, if the capacitance of the substrate voltage node becomes large and ~~contrary that of~~ the junction leakage current becomes small, the operational period of the substrate bias generator will become long. ~~In the meantime, as mentioned above, if~~ If the time when the semiconductor memory device is ~~stayed~~ held in the stand-by state ~~of the chip~~ is similar to or is shorter than the operational period of the substrate bias generator, during the stand-by state, the substrate bias generator doesn't need to ~~operate, however,~~ operate.

only during the active state, ~~it should operate~~. Thereby, it is possible to prevent ~~the~~ current consumption ~~under~~ the stand-by state ~~of the chip from being increased according to the substrate voltage~~. Accordingly, in the self refresh mode ~~to be refreshed by the period of the chip~~, since the time when the semiconductor memory device is ~~each stayed~~ in the stand-by state and the active state of the chip is determined by the ~~period generated in inside of~~ the chip, it is possible to know the time when the semiconductor memory device is ~~stayed~~ in the stand-by state. ~~Meantime, since~~ the time of the stand-by state is several ~~decades~~ to hundreds of microsecond(μs) and is similar to or is shorter than the operational period of the substrate bias generator, as described above, it is possible to apply a method which reduces the current by intercepting the operation of the substrate bias generator during the stand-by state. Further, since the time of the stand-by state is longer than that of the active state in the self refresh mode, if the operation of the substrate bias generator is stopped, the current consumption can be largely reduced during the stand-by state.

Returning to Fig. 2, when the self refresh mode is enabled and the signal ϕact is disabled, the substrate voltage level detecting controller 28 prevents the driving operation of the substrate voltage level detector 26 to thereby intercept the generation of the direct current within the substrate level detector 26, the controller 28 in the feed back manner inputting the self refresh enable signal ϕself, the active signal ϕact of the self refresh mode and the output signal of the substrate voltage level detector 26. Further, if the active state begins in the self refresh mode cycle, the signal ϕact is enabled. Thereby, the driving operation of the substrate bias generator and the substrate voltage level detecting operation of the substrate voltage level detector 26 are performed. Then, the output signal of the substrate voltage level detector 26 operates ~~continuously~~ the substrate bias generator ~~till the substrate~~ voltage VBB ~~is arrived~~ at the desired level, even if the semiconductor memory device is ~~stayed~~ in the stand-by state by inputting the output signal thereof to the controller 28 in the feed back manner. According to such a series of operations, if the semiconductor memory device enters into the self refresh mode, the driving operation of the substrate voltage level detector 26 is stopped during the stand-by state and is only performed in the cycle of the active state. Thereby, the substrate bias generator is enabled only until the substrate voltage VBB is boosted to the desired level. In the total operational

time of the self refresh mode, because the time when the substrate voltage level detector 26 is enabled is negligible enough ~~small~~ to be ignored, components of the direct current are eliminated in the operational current of the self refresh mode, the components of the direct current being generated in the substrate voltage level detector 26.

Fig. 3 is a detailed circuit view showing embodiments of the substrate voltage level detector 26 and its controller 28 according to the block construction of Fig. 2. In the construction of Fig. 3, the signal ϕself is generated according to conditions of inputs of a row address strobe signal $\overline{RAS}$ and a column address strobe signal $\overline{CAS}$, the row address strobe signal $\overline{RAS}$ and the column address strobe signal $\overline{CAS}$ being provided from the outside of the chip, i.e., the system. A process of generating the signal ϕself is known in the art such as is disclosed in Korean Patent Application No. 93-13276 entitled "A Circuit for Controlling the period of a Self Refresh Operation" filed 24 July 1993. As an active signal of the self refresh mode, the signal ϕact is generated in response to the inputs of the row address strobe signal $\overline{RAS}$ and the column address strobe signal $\overline{CAS}$. The controller 28 is comprised of a NOR gate 32 inputting the signals ϕself and ϕact through an inverter 30, a NAND gate 34 inputting an output signal of the substrate voltage level detector 26 and an output signal of the NOR gate 32, and an inverter 36 ~~reversely outputting~~ which inverts an output signal of the NAND gate 34. The substrate voltage level detector 26 is comprised of a PMOS transistor 38 whose source terminal is coupled to the power supply terminal Vcc and whose gate terminal is coupled to the output signal of the controller 28, a PMOS transistor 40 whose channel is formed between the PMOS transistor 38 ~~44~~ and ~~the~~ a connecting node 46 and whose gate terminal is coupled to the ground terminal Vss, a PMOS transistor 42 whose source terminal is coupled to ~~the ground terminal Vss~~ an NMOS transistor 44 and whose gate terminal is coupled to the substrate bias voltage VBB, ~~an~~ the NMOS transistor ~~40~~ 44 ~~whose channel is~~ having a channel formed between the PMOS transistor 42 and the ground terminal Vss and whose gate terminal is coupled to the power supply terminal Vcc, and an inverter 48 having an input terminal coupled to the connecting node 46 and generating the output signal of the substrate voltage level detector 26.

With reference to Fig. ~~4 being the~~ 4, which is an operational timing diagram of Fig. 3,

the operational characteristics of Fig. 3 will be explained hereinafter.

i) A state of a normal operation ~~that~~ wherein the self refresh mode is not performed, is described as follows. The signals ϕself and ϕact are each at the "low" level, ~~like an~~ as in interval T1 of Fig. 4, for example, the stand-by state of the normal operation. Therefore, the NOR gate 32 outputs the signal set to the "low" level by receiving the signal of the inverter 30 set to the "high" level. The NAND gate 34 is thus supplied with an output signal set to the "low" level and thereby outputs the signal set to the "high" level regardless of the voltage level of the node 24. The inverter 36 outputs the signal set to the "low" level by receiving the signal of the NAND gate 34 set to the "high" level. Accordingly, a control signal A of the PMOS transistor 38 becomes the "low" level, so that the substrate voltage level detector 26 is enabled to continuously perform the detecting operation of the substrate bias voltage VBB, the control signal A being an output signal of the inverter 36. ~~In the meantime, in~~ In the substrate bias generator of Fig. 2, it is well known that the detecting operation of the substrate voltage level detector 26 is stopped when the substrate bias voltage VBB is boosted to the desired level.

ii) With reference to an interval T2 of Fig. 4, the stand-by state of the self refresh mode, i.e., the substrate voltage level detector does not perform the detecting operation, is described as follows. As shown in Fig. 4, in case that the column address strobe signal $\overline{CAS}$ becomes active previous to the row address strobe signal $\overline{RAS}$ and is then input, if the self refresh mode entrance time $T_{self\text{-}in}$ goes by, the signal ϕself becomes the "high" level and another signal ϕact becomes the "low" level. Accordingly, the NOR gate 32 outputs the signal set to the "high" level by receiving the output signal of the inverter 30 set to the "low" level. Since the substrate bias voltage VBB is charged to the negative voltage level in the previous operation, the node 46 becomes the "low" level by the turning-on operation of the PMOS transistor 42, and the inverter 48 thus outputs the signal set to the "high" level. The NAND gate 34 outputs the signal set to the "low" level by receiving the signal of the NOR gate 32 set to the "high" level and the signal of the ~~NAND gate 34~~ inverter 48 set to the "high" level, respectively. The inverter 36 outputs the signal set to the "high" level by receiving the signal of the NAND gate 34 set to the "low" level. Accordingly, the signal A becomes the "high"

level and the PMOS transistor 38 is thus turned off. Thereby, the substrate voltage level detector 26 of Fig. 2 stops ~~the detecting operation~~ detecting of the substrate voltage VBB. As shown in Fig. 4, the interval T2 of the stand-by state ~~of Fig. 4~~ occupies most of the self refresh mode. Therefore, during the stand-by state of the self refresh mode, the operation of the substrate voltage level detector 26 is disabled, so that it is possible to reduce the current consumption.

iii) With reference to an interval T3 of Fig. 4, the active state of the self refresh mode is follows. The signal ϕself becomes the "high" level and also another signal ϕact becomes the "high" level. Thereby, the NOR gate 32 outputs the signal set to the "low" level by receiving the signal ϕact set to the "high" level. Then, the NAND gate 34 outputs the signal set to the "high" level regardless of the voltage level of the node 24 by receiving the signal of the NOR gate 32 set to the "low " level. The inverter 36 outputs the signal set to the "low" level by receiving the signal of the NAND gate 34 set to the "high" level. Thus, the signal A becomes the "low" level, so that the substrate voltage level detector 26 is enabled to continuously perform the detecting operation of the substrate bias voltage VBB.

The substrate voltage level detector 26 and its controller 28 of the substrate bias generator according to the present invention, as shown in Fig. 3, are the preferred embodiments based on the spirit of the present invention. However, it is well known to one skilled in the art that the ~~constructions of the~~ circuits can be constructed differently such as ~~differently embodied~~ in connection with the logic of the self refresh enable signal ϕself and the chip active enable signal ϕact.

As mentioned above, the substrate bias generator according to the present invention inputs the output signal of the substrate voltage level detector and ~~has the~~ includes a controller for controlling the switching operation of the substrate voltage level detector according to the input conditions of the self refresh enable signal ϕself and the active signal ϕact of the self refresh mode. Thereby, during the stand-by state of the self refresh mode, the generation of the direct current is prevented within the substrate voltage level detector and thus ~~there arises~~ an efficiency arises in that the current consumption can be reduced in the substrate bias generator.